CSE113: Parallel Programming March 7, 2022

- Topics:
 - Finish discussing HW 5
 - GPU programming

Instruction Buffer					
Warp Scheduler					
Dispatch Unit			Dispatch Unit		
Register File (16,384 x 32-bit)					
Core	Core	Core	Core	LD/ST	SFU
Core	Core	Core	Core	LD/ST	SFU
Core	Core	Core	Core	LD/ST	SFU
Core	Core	Core	Core	LD/ST	SFU
Core	Core	Core	Core	LD/ST	SFU
Core	Core	Core	Core	LD/ST	SFU
Core	Core	Core	Core	LD/ST	SFU
Core	Core	Core	Core	LD/ST	SFU

Announcements

- HW 4 was due on Friday
- HW 5 was released on Friday (technically Saturday AM... apologies!)
 - Please get started on it ASAP so that we can sort out technical issues sooner rather than later
 - Designed to be lighter than the previous homeworks.
 - Due by midnight the day before the final (March 16)
- HW 3 grades are released
 - Let us know ASAP if there are issues
 - If you are missing grades that should be there, definitely let us know!

Announcements

- Final is on March 17
 - I will release it by 8 AM, and you will have until midnight to turn it in
 - If you want to allocate time for it, our official final time is 4 PM to 7 PM
 - Same rules at the midterm:
 - Do not discuss with class mates
 - Do not google specific answers or ask questions on forums
 - You can use your notes, the slides, and the internet to google for general concepts.
 - worth 30% of your grade.

Announcements

- SETs are out!
 - Please fill them out; I know they are a pain and we're all busy
 - But it has an outsized effect on classes like this one
 - New class
 - New content
 - New professor
 - I would love to help

Quizes

- We will cancel quizzes for the rest of the quarter;
 - It's a busy time for everyone and I want to make sure we can support you in HW 5 as much as possible.
 - If you think of good quiz questions let me know!

Review

Homework 5

Homework 5- requirements

• The browser

- Google Chrome Canary
- (if you have linux, Google Chrome Dev should work)
- Why do we need the Canary?
 - WebGPU is new and support is inconsistent on main (Although it is officially supported)
 - Perhaps more interesting is the shared array buffer.
 - Make sure you navigate to http://localhost:8000

Homework 5 - requirements

Node.js and local webservers

- Permission issues
 - you can try running with sudo (generally considered bad)
 - a stack overflow thread with installation options

Javascript

- logging
- variables
- objects
- shared array buffers

What does the solution look like?

• Demo

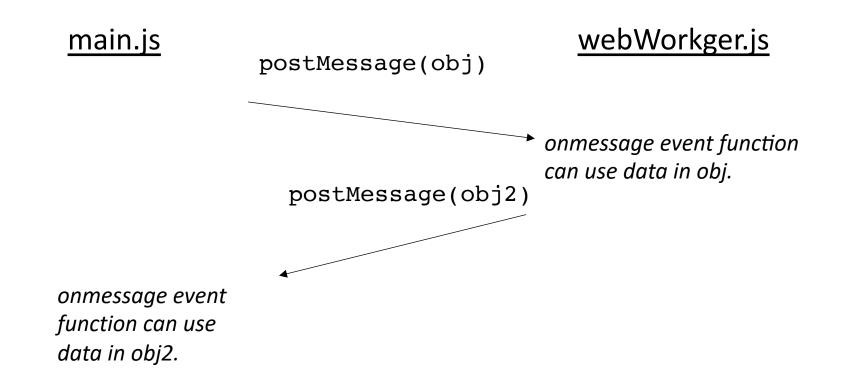
New material

Web Workers demo

Overview: Web Workers

- Create a new worker with a new .js file (this is done for you)
 - Nothing happens on creation
- File contains an onmessage event function
- Main file calls postMessage to start the thread along with an object argument.
- Worker sends a message back to the main file (postMessage), it can catch the data with an onmessage event.

Overview: Web Workers



Your Homework (part 1 and part 2)

- part 1 you only modify the Web Worker.
 - You are given code to do all of the Web Worker interface (sending message, posting messages, etc).
 - You just need to update the particles every timestep
- part 2 you need to modify the Web Worker for it to be multithreaded
 - Most of your web worker from part 1 will apply.
 - You will need extra arguments
 - You will need to modify main.js to launch multiple web workers and figure out how to make sure they are all finished before drawing and calling the next iteration of updates.

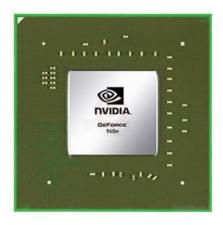
Your Homework (part 3)

- part 3
 - You will only modify the GPU kernel code.
 - WebGPU simply has too much boiler plate.
 - We will discuss CUDA mappings to WebGPU on Wednesday

On to the GPU part of the lecture!

Programming a GPU

The GPU in my PhD laptop



Nvidia 940m 1.8 Billion transistors 33 TDP Est. \$130 Fight!



The CPU in my professor workstation



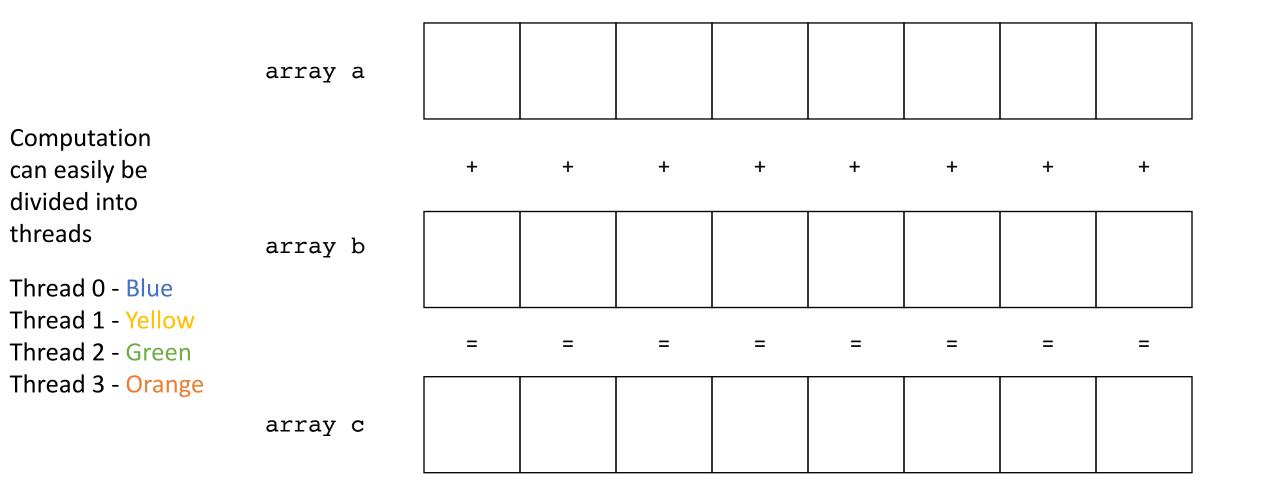
Intel i7-9700K 2.16 Billion transistors 95 TDP Est. \$316

https://www.techpowerup.com/gpu-specs/geforce-940m.c2648 https://www.alibaba.com/product-detail/Intel-Core-i7-9700K-8-Cores_62512430487.html https://www.prolast.com/prolast-elevated-boxing-rings-22-x-22/

Programming a GPU

• The problem: Vector addition

Embarrassingly parallel



Programming a GPU

- The problem: Vector addition
- Who can do it faster?

Lets set up the CPU

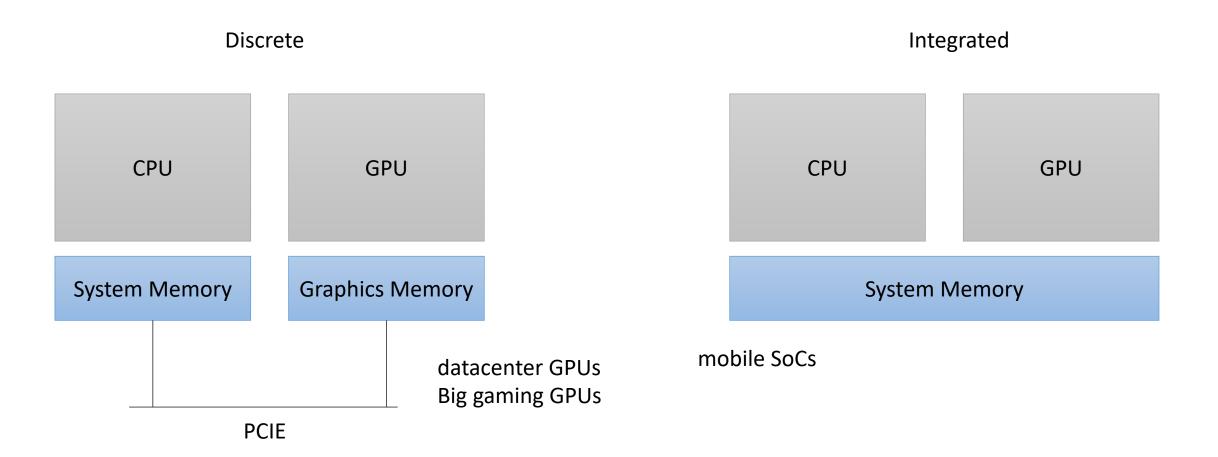
• CPU code

Now for the GPU

• Its going to take a bit of work....

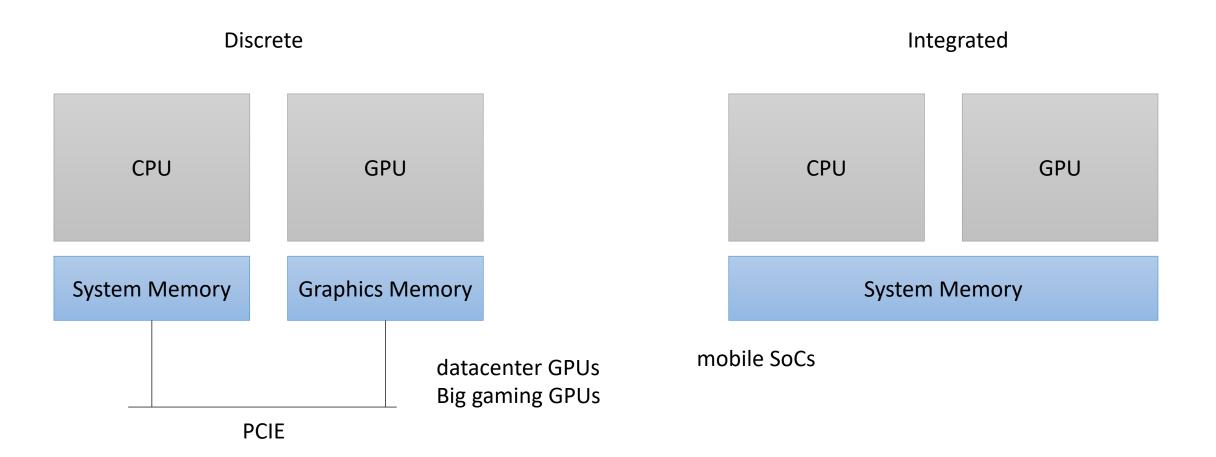
• We need to allocate and initialize memory

• GPUs come in two flavors



Pros and cons of each?

• GPUs come in two flavors

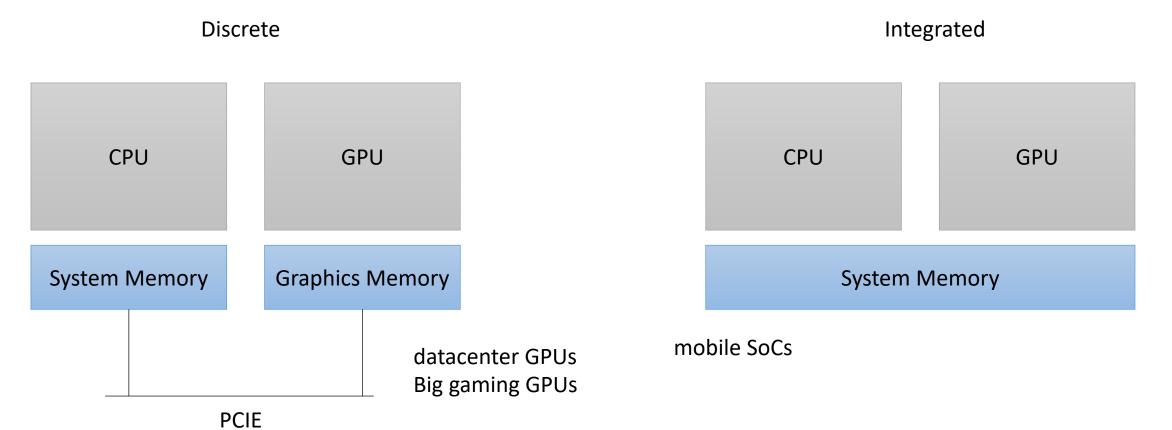


GPUs come in two flavors

Pros and cons of each?

* Different types of memory for discrete

- * Swappable for discrete
- * More energy efficient for integrated
- * Better memory utilization for integrated
- * More efficient communication between CPU and GPU



• GPUs come in two flavors

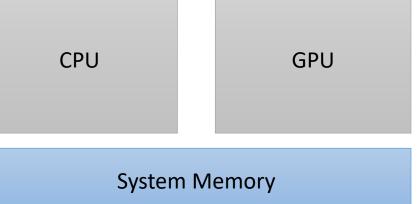
Discrete

CPU GPU **Graphics Memory** System Memory PCIE

Although mobile GPUs share the system memory, Most still require you to program as if they didn't have shared memory.

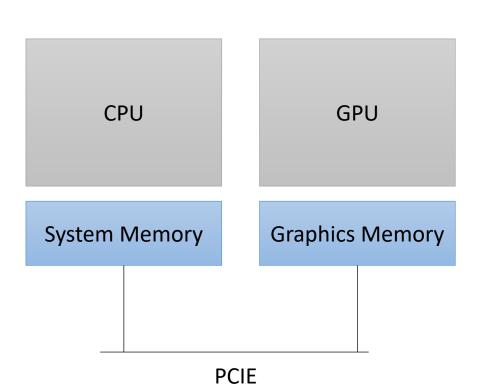
Why?





• GPUs come in two flavors

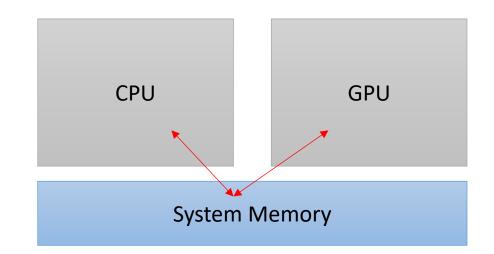
Discrete



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Why?



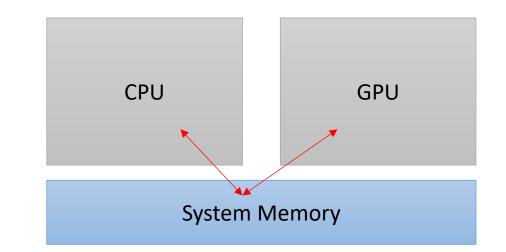


• GPUs come in two flavors

Although mobile GPUs share the system memory, Most still require you to program as if they didn't have shared memory.

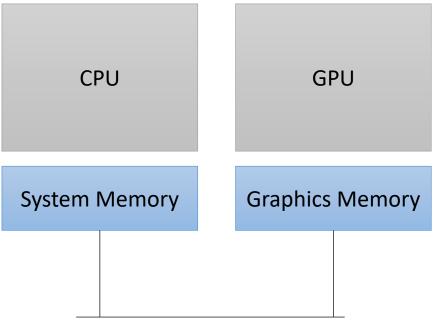
Why?



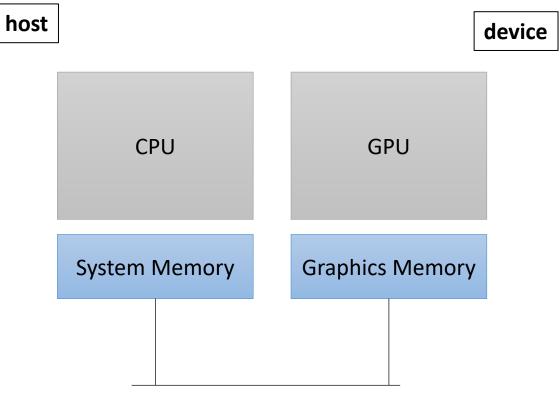


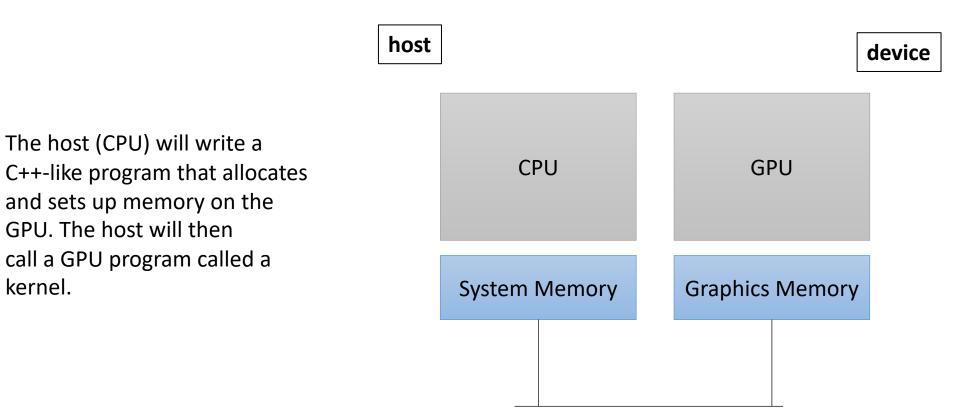
In many cases, CPU-GPU communication is not fully supported coherence, fences, and RMWs might now be supported.



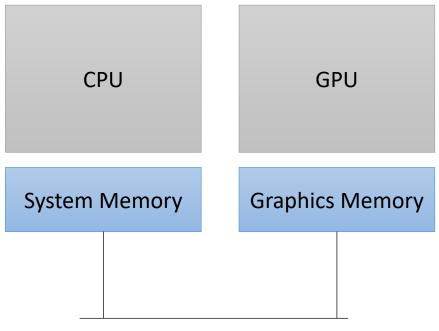


PCIE





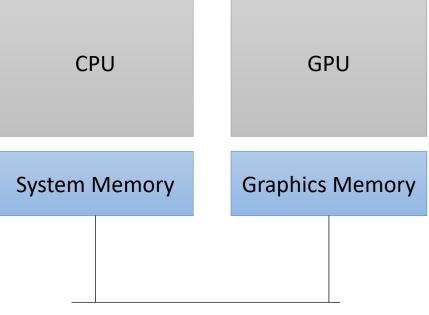
How do we allocate memory on a CPU?



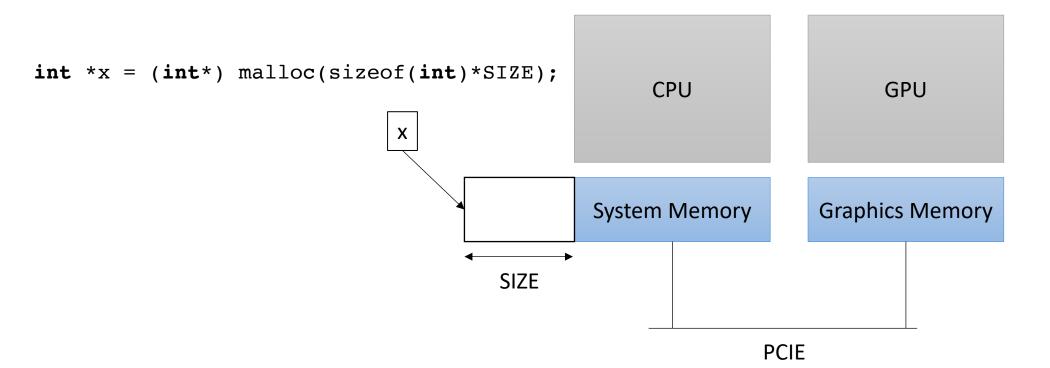
How do we allocate CPU memory on the host?

• Our heterogeneous, parallel, programming model

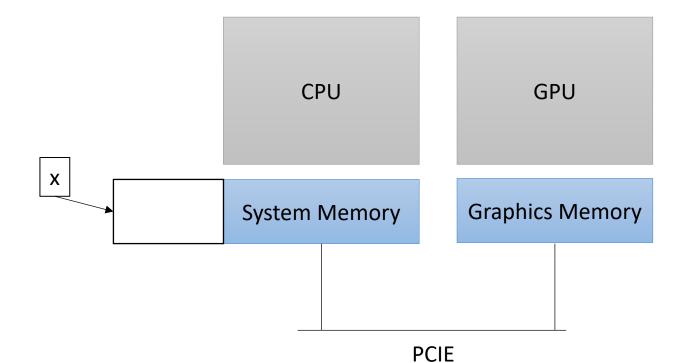
int *x = (int*) malloc(sizeof(int)*SIZE);



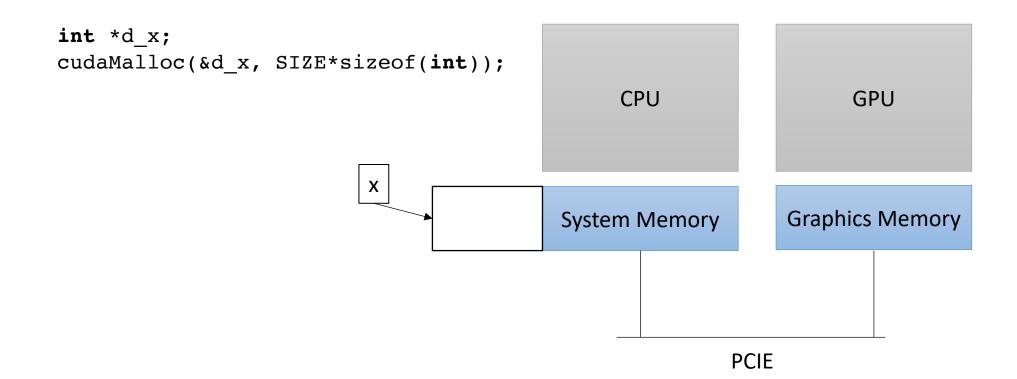
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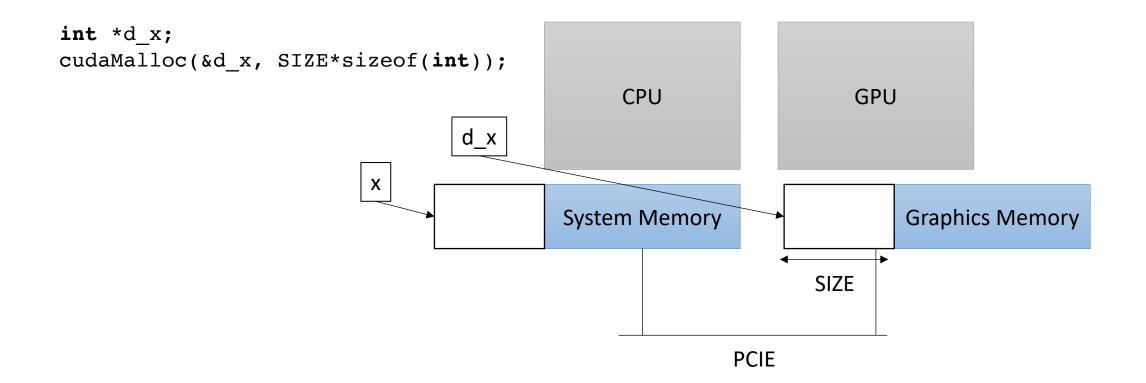
We need to allocate GPU memory on the host



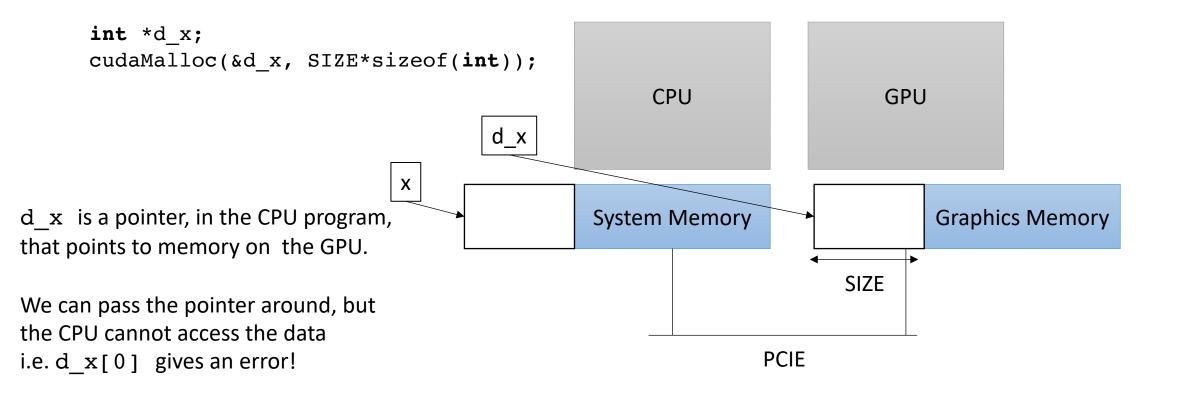
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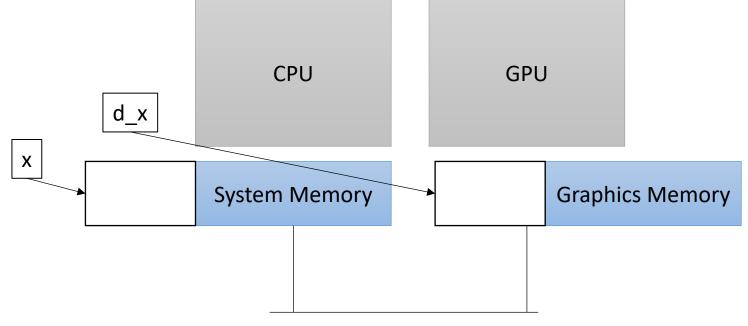


We need to allocate GPU memory on the host



We need to allocate GPU memory on the host

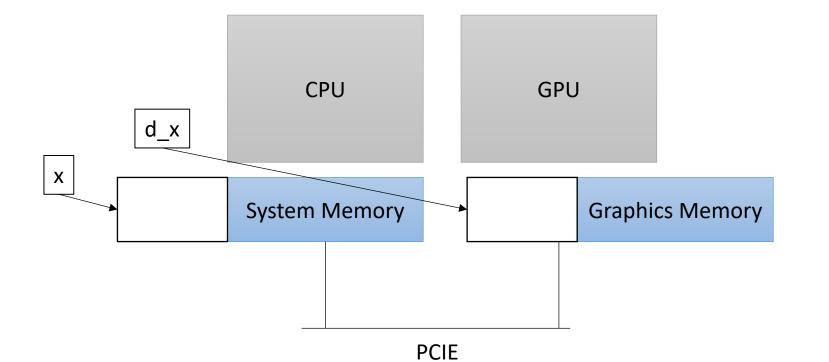




• Our heterogeneous, parallel, programming model

If we can't access d_x on the CPU, how do we initialize the memory?

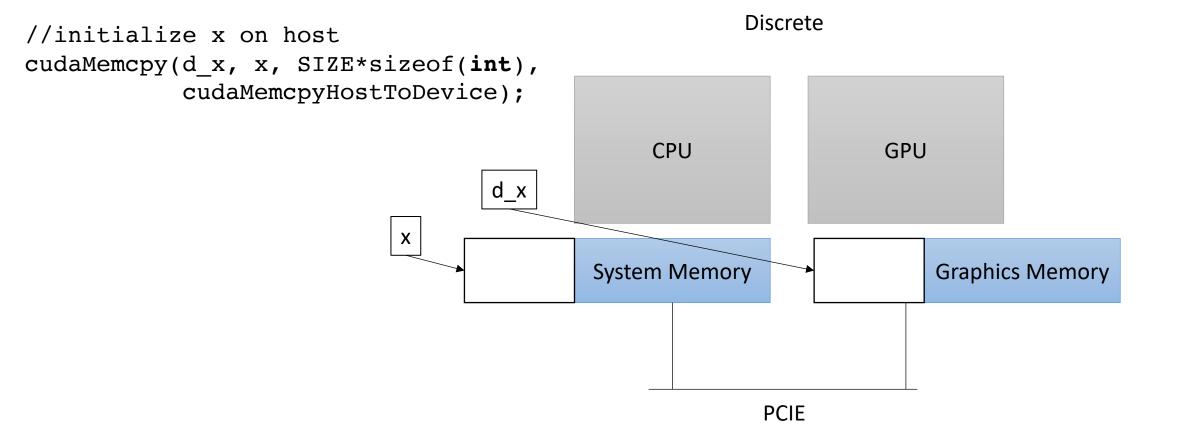
GPU has no access to input devices e.g. disk



• Our heterogeneous, parallel, programming model

If we can't access d_x on the CPU, how do we initialize the memory?

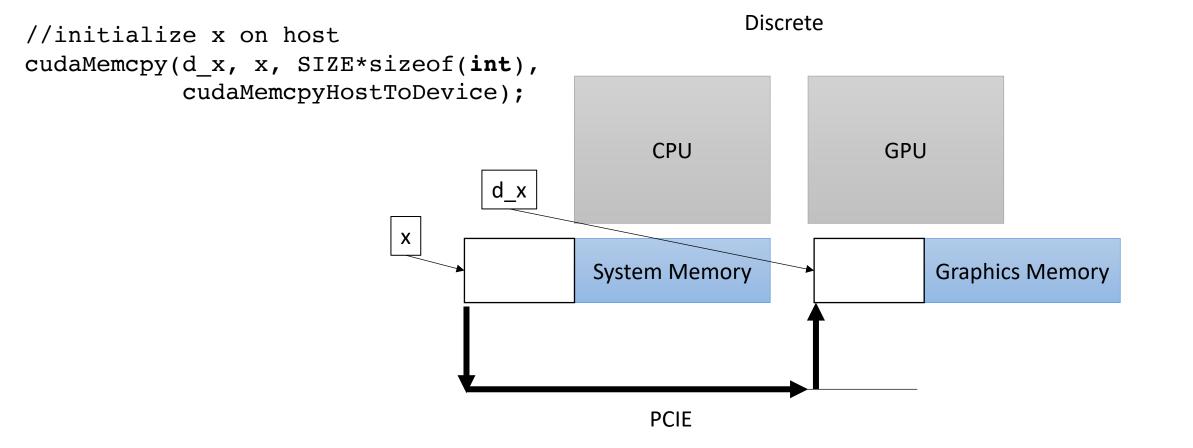
GPU has no access to input devices e.g. disk



• Our heterogeneous, parallel, programming model

If we can't access d_x on the CPU, how do we initialize the memory?

GPU has no access to input devices e.g. disk



- Write a special function in your C++ code.
 - Called a Kernel
 - Use the new keyword ___global___
 - Keywords in
 - OpenCL __kernel
 - Metal kernel
- Write it how you'd write any other function

```
__global___ void vector_add(int * a, int * b, int * c, int size) {
    for (int i = 0; i < size; i++) {
        a[i] = b[i] + c[i];
    }
}</pre>
```

```
__global___ void vector_add(int * a, int * b, int * c, int size) {
   for (int i = 0; i < size; i++) {
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```

calling the function

```
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   }
}</pre>
```

calling the function

What in the world? special new CUDA syntax. We will talk more soon

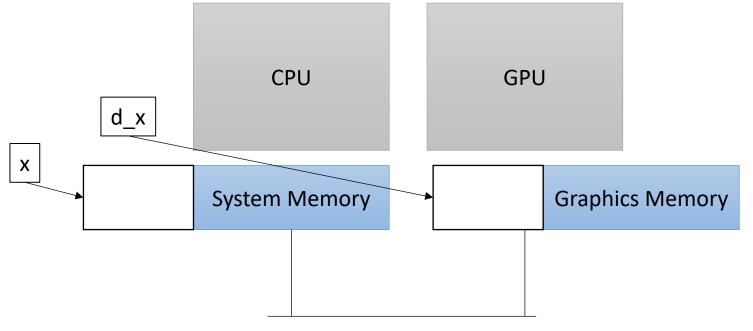
```
__global___ void vector_add(int * d_a, int * d_b, int * d_c, int size) {
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        d_a[i] = d_b[i] + d_c[i];
    }
}</pre>
```

Pass in pointers to memory on the device

calling the function

• Our heterogeneous, parallel, programming model

Remember, GPU needs to access its own memory

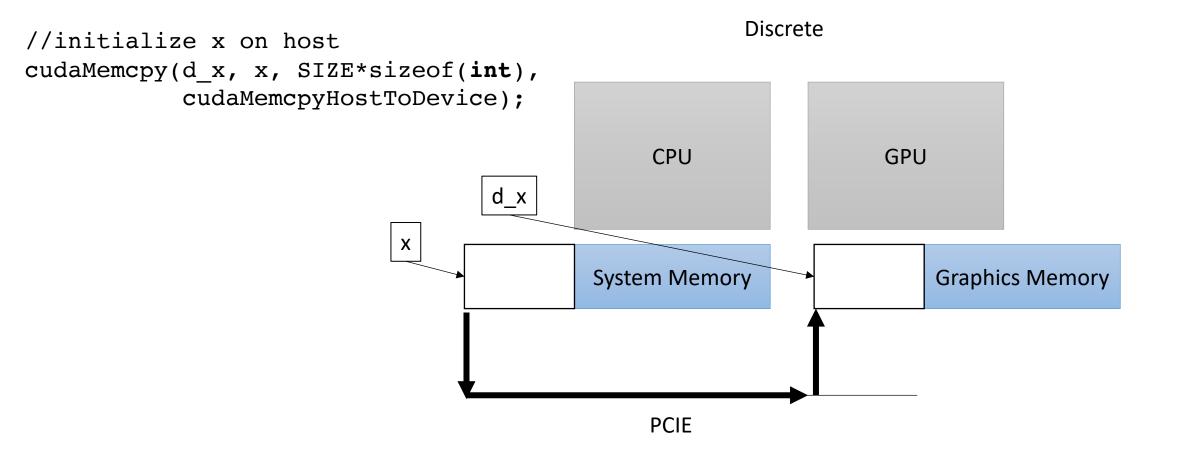


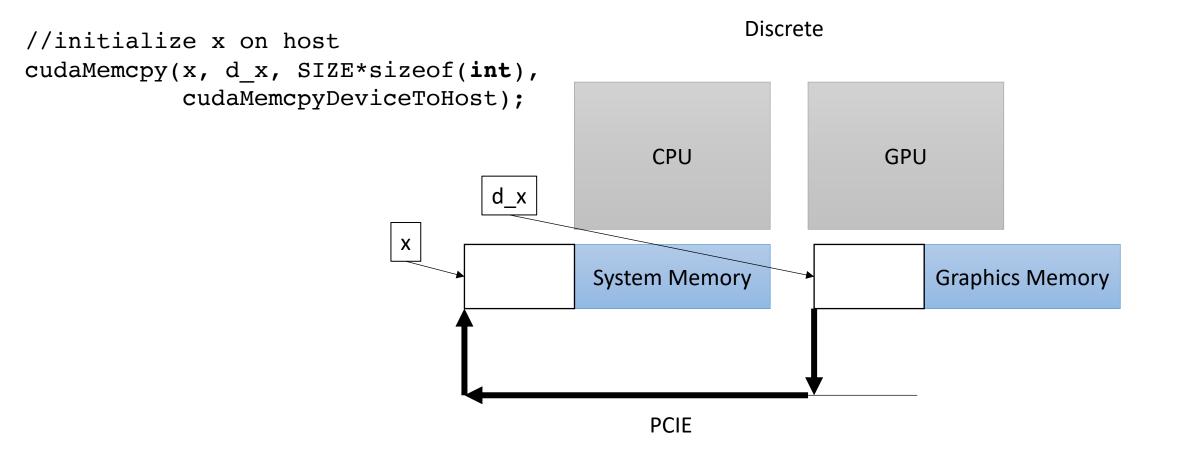
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   for (int i = 0; i < size; i++) {
     d_a[i] = d_b[i] + d_c[i];
   }
}</pre>
```

Constants can be passed in regularly

calling the function

Are we ready to run the program? What are we missing?





Finally, we can run the GPU program!

Lets see what all the hype is about



It didn't do so well...

- Lets look at some GPU documentation.
- The Maxwell whitepaper shows a diagram of one of the GPU cores

Instruction Buffer								
Warp Scheduler								
Dispatch Unit			Dispatch Unit					
Register File (16,384 x 32-bit)								
Core	Core	Core	Core	LD/ST	SFU			
Core	Core	Core	Core	LD/ST	SFU			
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Core	Core	Core	Core	LD/ST	SFU			
Core	Core	Core	Core	LD/ST	SFU			
Core	Core	Core	Core	LD/ST	SFU			
Core	Core	Core	Core	LD/ST	SFU			
Core	Core	Core	Core	LD/ST	SFU			

https://www.techpowerup.com/gpu-specs/docs/nvidia-gtx-980.pdf

woah, 32 cores!

We should parallelize our application!

Instruction Buffer								
Warp Scheduler								
Dispatch Unit			Dispatch Unit					
Register File (16,384 x 32-bit)								
Core	Core	Core	Core	LD/ST	SFU			
Core	Core	Core	Core	LD/ST	SFU			
Core	Core	Core	Core	LD/ST	SFU			
Core	Core	Core	Core	LD/ST	SFU			
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https://www.techpowerup.com/gpu-specs/docs/nvidia-gtx-980.pdf

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```

calling the function

```
__global___ void vector_add(int * d_a, int * d_b, int * d_c, int size) {
    for (int i = 0; i < size; i++) {
        d_a[i] = d_b[i] + d_c[i];
    }
}</pre>
```

calling the function

vector_add<<<1,32>>>(d_a, d_b, d_c, size);

number of threads to launch the program with

```
__global___ void vector_add(int * d_a, int * d_b, int * d_c, int size) {
    int chunk_size = size/blockDim.x;
    int start = chunk_size * threadIdx.x;
    int end = start + end;
    for (int i = start; i < end; i++) {
        d_a[i] = d_b[i] + d_c[i];
    }
}</pre>
```

calling the function

number of threads

```
vector_add<<<1,32>>>(d_a, d_b, d_c, size);
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```

calling the function

vector_add<<<1,32>>>(d_a, d_b, d_c, size);

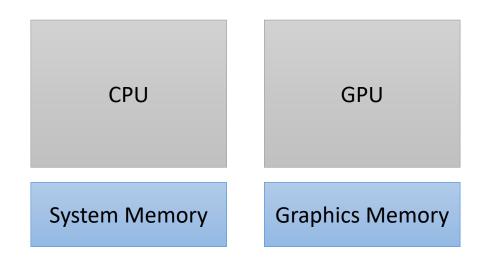
number of threads thread id

Lets try it! What do we think?



Getting better but we have a long ways to go!

GPU Memory

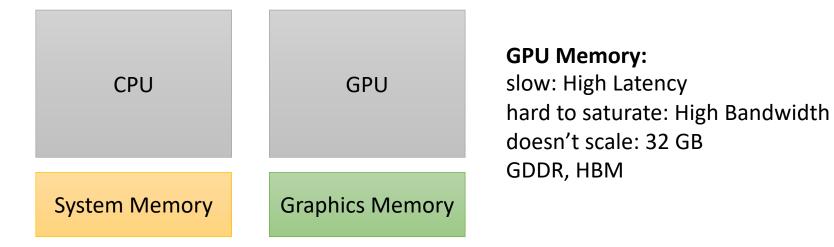


GPU Memory

CPU Memory:

Fast: Low Latency Easily saturated: Low Bandwidth Scales well: up to 1 TB DDR

2-lane straight highway driven on by sports cars



Different technologies

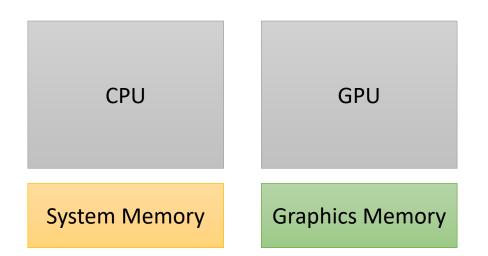
16-lane highway on a windy road driven by semi trucks

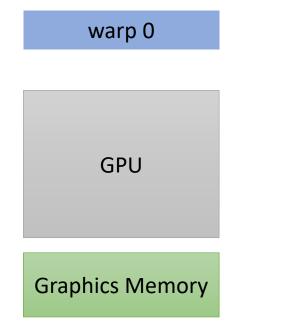
GPU Memory

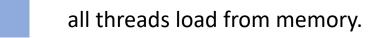
bandwidth: ~**700 GB/s** for GPU ~**50 GB/s** for CPUs

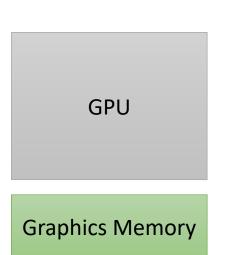
memory Latency:~600 cycles for GPU memory~200 cycles for CPU memory

Cache Latency: ~**28** cycles for L1 hit for GPU ~**4** cycles for L1 hit on CPUs

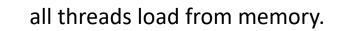




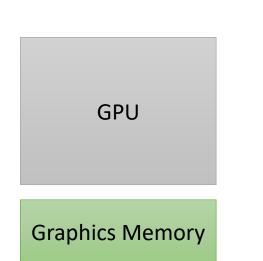




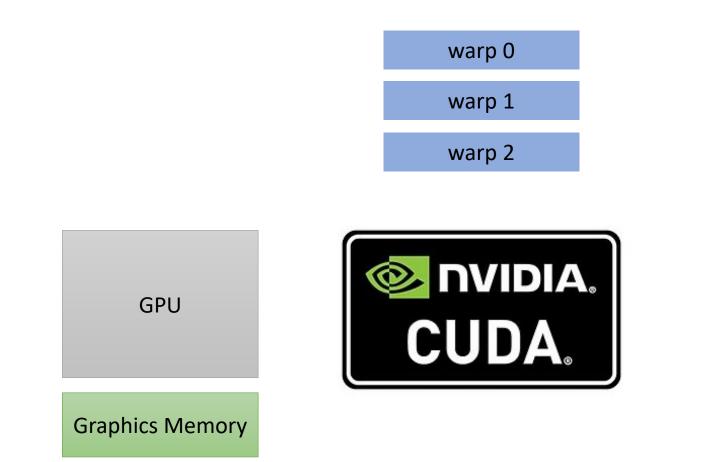
warp 0



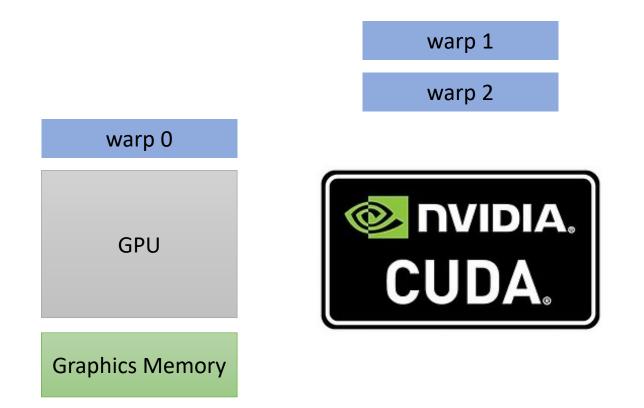
600 cycles!

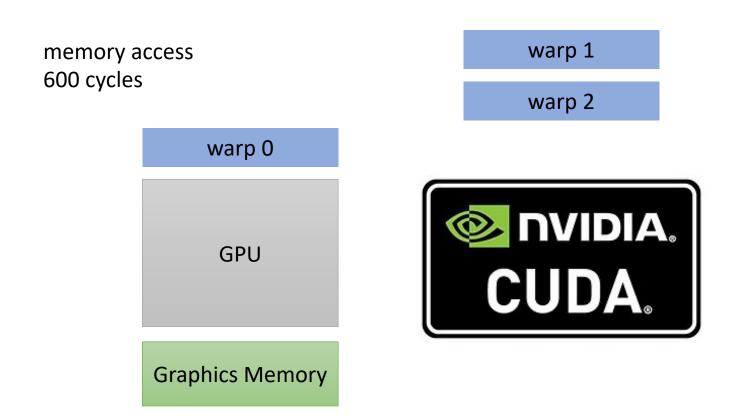


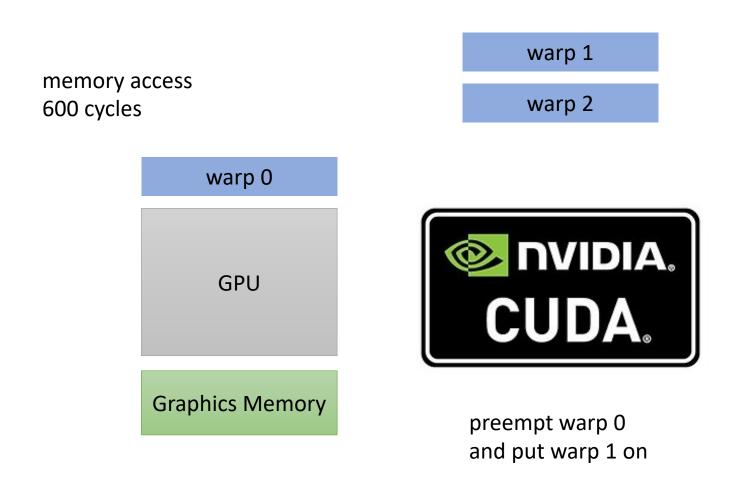
warp 0

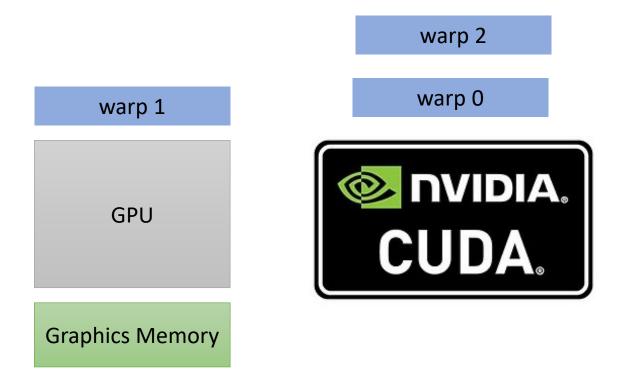


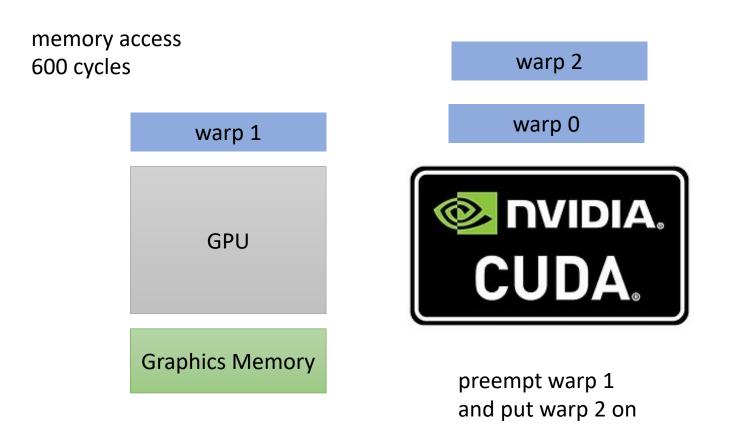
We can hide latency through preemption and concurrency!

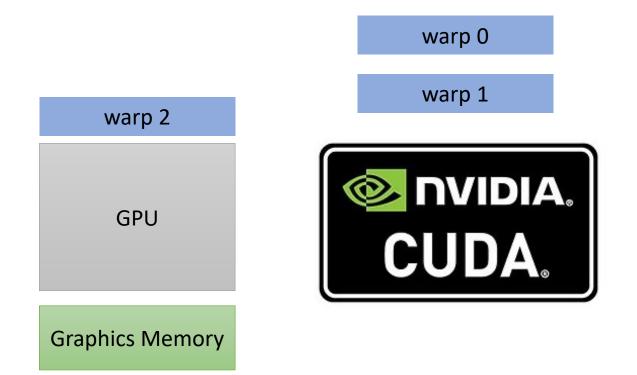


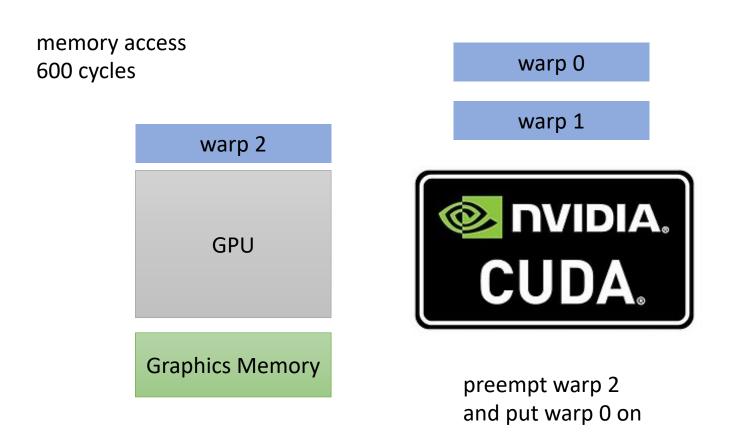




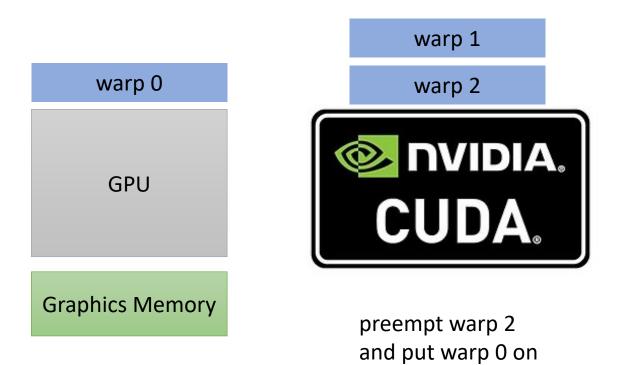




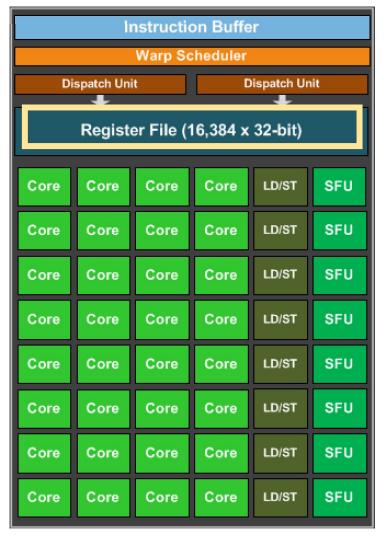




Hey, my memory has arrived!



But wait, I thought preemption was expensive?

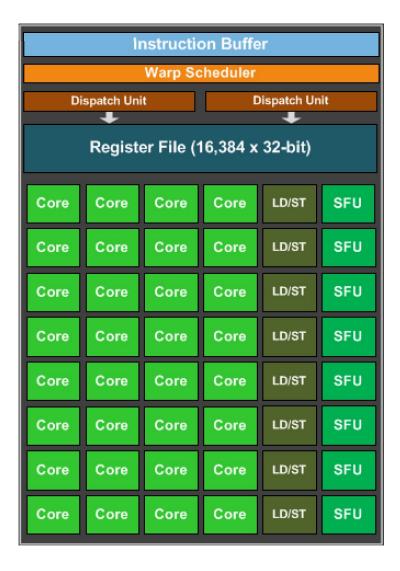


But wait, I thought preemption was expensive?

Registers all stay on chip

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Warp Scheduler					
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But wait, I thought preemption was expensive? dedicated scheduler logic



But wait, I thought preemption was expensive?

bound on number of warps: 32

Go back to our program

```
__global___ void vector_add(int * d_a, int * d_b, int * d_c, int size) {
    int chunk_size = size/blockDim.x;
    int start = chunk_size * threadIdx.x;
    int end = start + end;
    for (int i = start; i < end; i++) {
        d_a[i] = d_b[i] + d_c[i];
    }
}</pre>
```

calling the function

Lets launch with 32 warps

```
vector_add<<<1,32>>>(d_a, d_b, d_c, size);
```

Go back to our program

```
__global___ void vector_add(int * d_a, int * d_b, int * d_c, int size) {
    int chunk_size = size/blockDim.x;
    int start = chunk_size * threadIdx.x;
    int end = start + end;
    for (int i = start; i < end; i++) {
        d_a[i] = d_b[i] + d_c[i];
    }
}</pre>
```

calling the function

Lets launch with 32 warps

```
vector_add<<<1,1024>>>(d_a, d_b, d_c, size);
```

Concurrent warps

Lets try it! What do we think?

Concurrent warps

Lets try it! What do we think?



Getting better!

See you on Wednesday!

- We will continue optimizing the GPU program!
- Get started on HW 5!